What is claimed is:

1. An apparatus, comprising:

a semiconductor or dielectric wafer having front and back surfaces;

a sequence of alternating conductive and dielectric layers formed over said front surface, the sequence including top and middle conductive layers, the middle conductive layer being closer to said wafer than the top conductive layer; and

a bottom conductive layer; and

wherein the middle conductive layer has a substantially right cylindrical cavity that crosses a width of the middle conductive layer, the top and bottom conductive layers cap respective first and second ends of the cavity; and

wherein the top conductive layer includes a hole that forms a first access port to the cavity; and

wherein the wafer includes a via through the width of the wafer, the via provides access to the cavity via the back surface of the wafer, and the wafer is substantially thicker than the sequence of layers.

2. The apparatus of claim 1, wherein the wafer is ten or more times as thick as the sequence of layers.

3. The apparatus of claim 1, wherein the sequence comprises the bottom conductive layer that caps the second end of the cavity.

4. The apparatus of claim 1, wherein the wafer comprises a conductive region that forms the bottom conductive layer that caps the second end of the cavity.

5. The apparatus of claim 1, wherein the cavity has a height that is less than about 10 microns.

6. The apparatus of claim 2, wherein the conductive layers and conductive material comprise metal, heavily doped semiconductor, or silicide.

7. The apparatus of claim 2, wherein one dielectric layer of the sequence electrically insulates the middle conductive layer from the top conductive layer and another dielectric layer of the sequence electrically insulates the middle conductive layer from the bottom conductive layer.

8. The apparatus of claim 1, wherein the cavity has a circular cross section.

9. The apparatus of claim 1, further comprising an ion detector located to detect ions ejected from the via.

10. The apparatus of claim 9, further comprising an electron gun located to ionize molecules traveling towards the first access port.

11. The apparatus of claim 1,

wherein the middle conductive layer includes a second cylindrical cavity that crosses the width thereof, the top conductive layer capping a first end of the second cavity, and the bottom conductive layer capping a second end of the second cavity; and

wherein a second hole through the top conductive layer forms a first access port to the second cavity; and

wherein a via through the width of the wafer and provides access to the second cavity via the back surface of the wafer.

12. A method for fabricating an ion trap, comprising:

forming a sequence of alternating conductive and dielectric layers on a planar front surface of a dielectric or semiconductor wafer;

etching a right cylindrical cavity through one conductive layer of the sequence to produce a central electrode of the ion trap;

forming another conductive layer over said central electrode;

etching a hole through said another conductive layer to produce a first end cap electrode of the cavity, the hole forming an access port to said cavity;

etching through a back surface of said wafer to produce a via that provides an access to a second end cap electrode for said cavity, the second end cap electrode including one of another conductive layer of the sequence and a conductive region of the wafer.

13. The method of claim 12, further comprising:

depositing a sacrificial material to fill said cavity and producing a flat top surface over an end of the cavity prior to performing the forming another conductive layer; and

etching said sacrificial material from said cavity after performing the forming another conductive layer.

14. The method of claim 12, further comprising:

etching the one of another conductive layer of the sequence and a conductive region of the wafer to form a second access port to the cavity.

15. The method of claim 12, wherein the wafer has a thickness that is ten or more times as larger as the height of the cavity.

16. The method of claim 12, wherein the cavity has a height of 100 micrometers or less.

17. The method of claim 12, wherein the second end cap electrode is another conductive layer of the sequence.

18. The method of claim 12, wherein the conductive layers are metallic, heavily doped semiconductor, or silicide.

19. The method of claim 17, wherein forming a sequence further comprises:

forming the another conducting layer of the sequence over a surface of the wafer;

forming one dielectric layer on the another conducting layer of the sequence; and

then, forming said one conductive layer of the sequence on said one dielectric layer.

20. The method of claim 12, wherein the cavity has one of a circular cross section and an oval cross section.